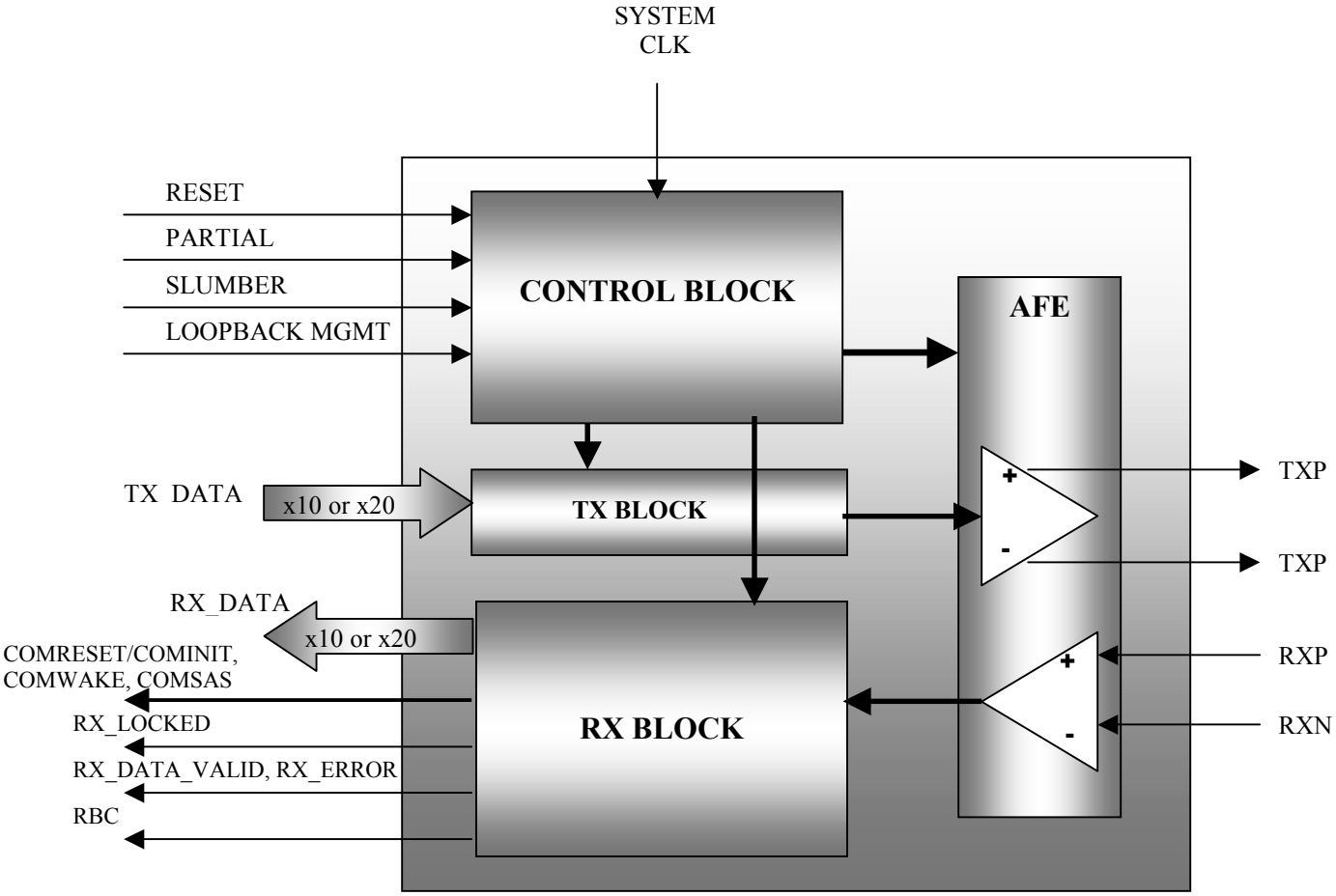
SMS6000 Serial ATA (SATA) PHY TRANSCEIVER IP

(Also supports Serial Attached SCSI SAS and Compliant with SATA PHY Interface Specification, SAPIS)



MAIN FEATURES

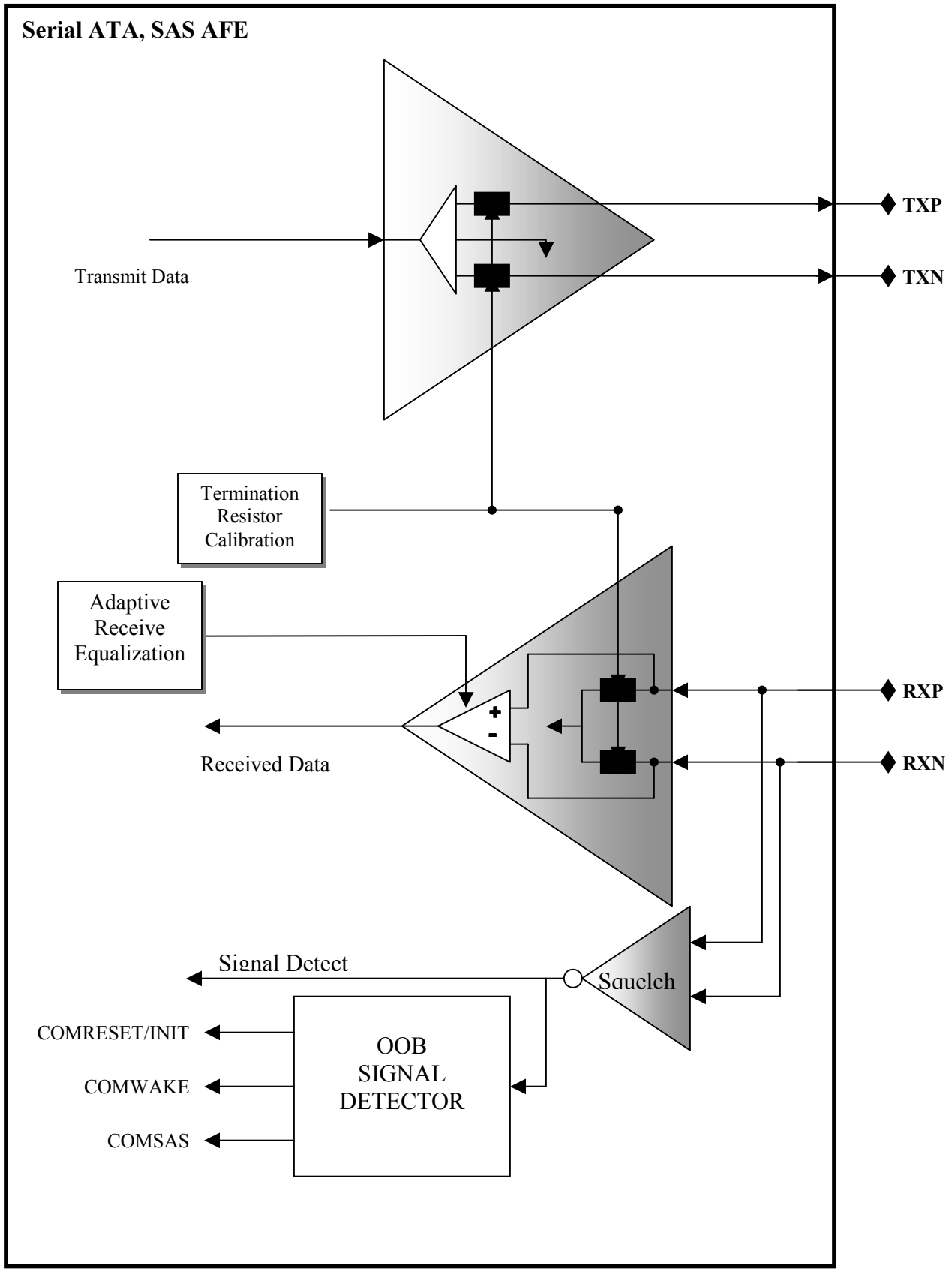
- Supports 1.5 Gb/s (Gen 1) and 3.0 Gb/s (Gen 2) serial data rate
- Compatible with Serial ATA II
- Utilizes 10-bit or 20-bit parallel interface to transmit and receive Serial ATA data
- Data and clock recovery from serial stream on the SATA bus
- Optional 8b/10b encode/decode and error indication
- Near-End and Far-End Loop-back Support
- Embedded Bit Error Rate Testing Through PBRS generation and detection
- Supports HOST and DEVICE controller applications
- OOB Signal Detection for COMWAKE, COMRESET/COMINIT and COMSAS
- COMMA & Squelch Detect Support
- Power Management Support for Slumber and Partial PM Modes.
- Calibrated Internal RX, TX Termination Resistors
- Support for Serial Attached SCSI SAS Mode
- Compliant with SATA PHY Interface Specification (SAPIS)
- Full low cost, low power CMOS Implementation
- Requires No external loop filter Capacitor

GENERAL DESCRIPTION

SMS6000 is a fully integrated CMOS transceiver that handles the low level Serial ATA protocol and signaling. It contains all necessary Clock synthesis, Clock Recovery, Serializer, Deserializer, Comma detect for 8B/10B encoded data and Frame alignment functionalities. Digital controller interface is realized with a 10-bit parallel operation (Optional 20-bit Interface) that allows use of 150 MHz (300 MHz) reference Clock. The transceiver includes Signal Detect, COMRESET/COMINIT and COMWAKE Out-of-Band capability compliant with Serial ATA Specification requirements in addition to COMSAS Out-of-band Signal detection capability required by the Serial Attached SCSCI (SAS). **SMS6000** complies with the latest version of the SAPIS standard both as a PHY Core IP and for discrete Transceiver implementations.

SMS6000 implements the full requirements of Serial ATA 1.0a specification in terms of Power Management and Loopback functionality. Both Partial and Slumber power management modes are fully supported both in the digital portion and the AFE of the PHY for maximum power efficiency. Also all the Loopback functions such as Near-End-Loopback and Far-End-Loopback are supported in addition to proprietary Loopback implementations for functional testing.

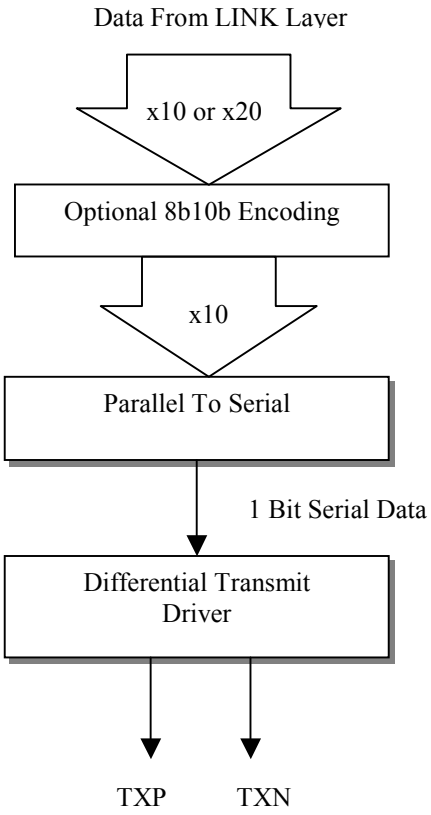
SMS6000 does not require any external Loop filter capacitor(s) for clock Synthesis PLL or Clock recovery circuitry making it immune to PCB related noise typically encountered, and provides a completely integrated solution.



Transmit Block:
Transmitter Block includes Calibrated Terminations, an Optional 8b/10b Encoder, Parallel To Serial Converter and Transmit Differential Driver.

The Transmit Data is received from the Controller over TX_DATA bus in 10 or 20 bit widths when TX_ENABLE is active. There is an optional 8b10b Encoder. The Parallel Data is converted to serial mode and driven through the AFE Differential Transmit drivers to the TXP, TXN pins.

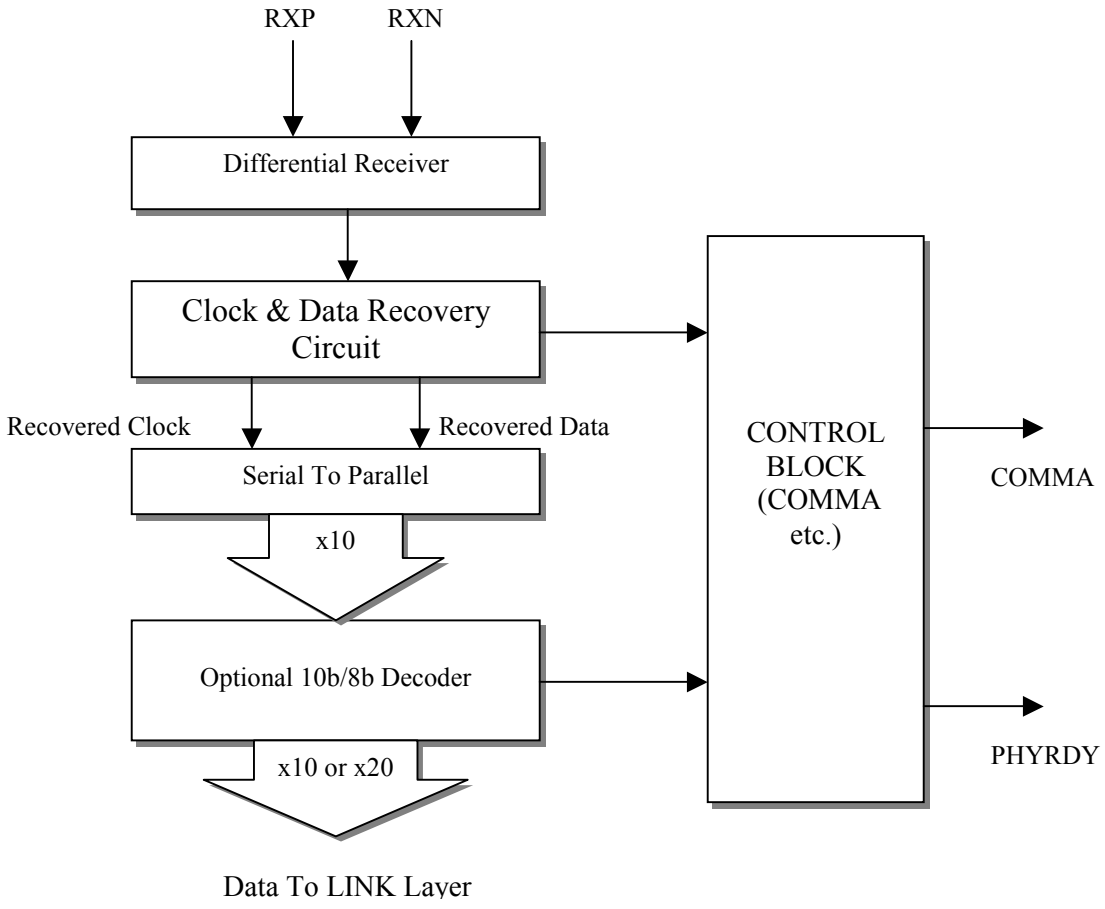
The Transmit Block also includes integrated/calibrated Termination Resistor and Common Mode Bias Controls.



Receiver Block:
Receiver Block includes Differential Receiver, Clock and Data Recovery Blocks, Comma Detect Circuit, Serial To Parallel Converter, Optional 10b/8b Decoder, Squelch Detect, COMRESET/COMINIT and COMWAKE support. Also COMSAS OOB signal detection is supported for SAS.

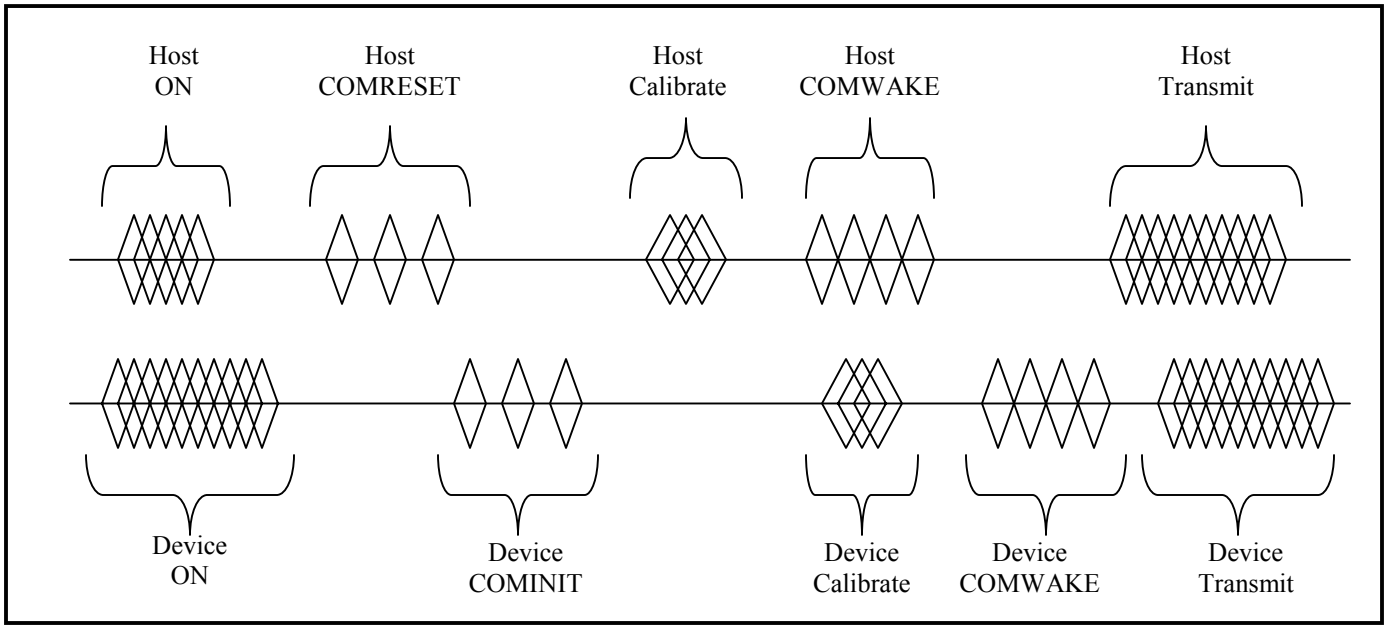
The Differential Recevie Data On RXP, RXN pins are converted to internal signalling format by the differential receiver. In AFE there is also a Squelch Detector which detects signalling level being in the normal range. When there is normal voltage level on the line, Clock & Data Recovery circuits generate Recovered Clock and Data in Serial format. After the clock locking and bit locking is established, the received data is then converted to parallel and Symbol alignment is established by detecting COMMA symbols.

There is an optional 10b8b Decoder before the Controller which can be configured if required.

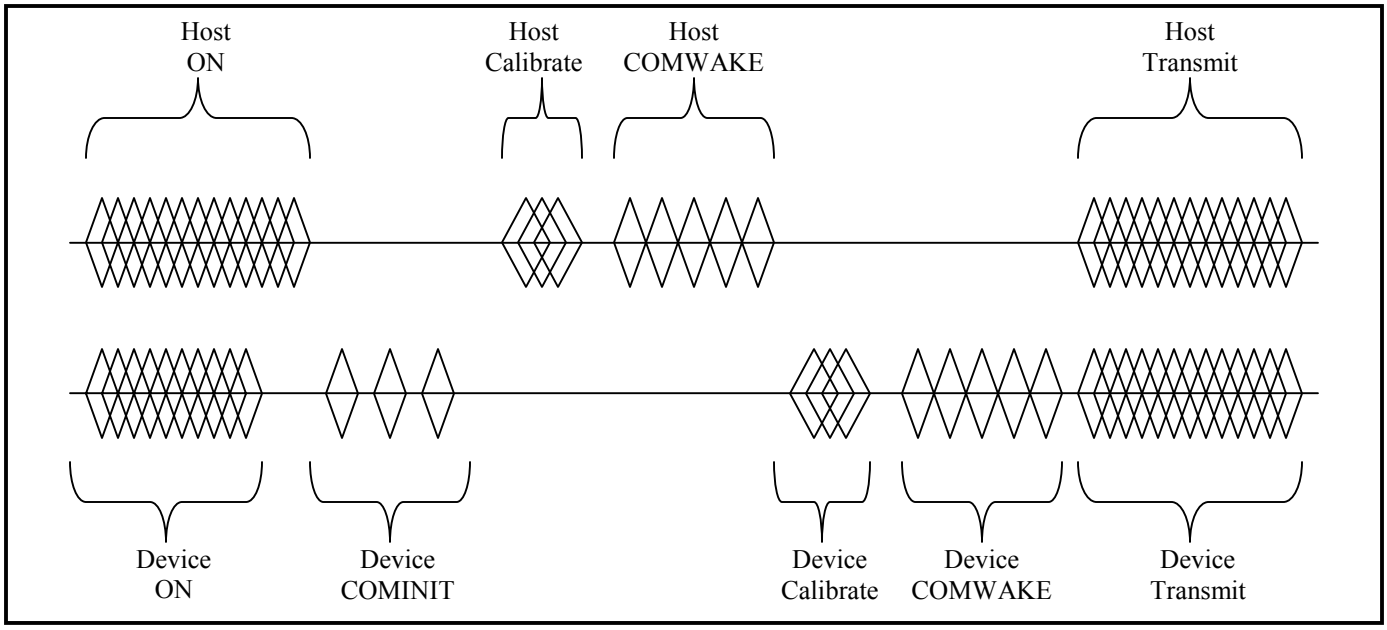


Compliant with Serial ATA Final 1.0 Specification and current SATA PHY Interface Specification (SAPIS).

Out-of-Band Signaling:
The PHY supports detection of COMWAKE, COMRESET, COMINIT and COMSAS Out-of-Band signals. COMWAKE, COMRESET, COMINIT and COMSAS signaling is achieved by transmission of 160 Gen1 UI bursts of ALIGN primitives each separated by idle periods at common mode levels. For COMWAKE the idle period is 160 Gen1 UI periods. For COMINIT and COMRESET, the idle period is 480 Gen1 UI periods. For COMSAS the idle period is 1440 Gen1 UI periods.



COMRESET Sequence



COMINIT Sequence

Signal Descriptions

RX Block Signals

Signal Name	Direction	Signal Description
RXP, RXN	Input	The differential inputs to the PHY
RX_DATA_VALID	Output	Used for flow control. High Indicates RX_DATA outputs are valid.
RX_DATA	Output	Recovered 10b Data from PHY. RX_DATA Bus can be either 10 bits or 20 bits in size depending on configuration.
K28_5_DETECT	Output	Comma detected at RX_DATA. COMMA is high when K28.5 symbol of either disparity is present on RX_DATA bus.
RX_LOCKED	Output	Indicated Bit and Symbol Lock. It goes high while three conditions are met: 1. The differential signal at inputs RXP, RXN exceeds the Squelch Detector Threshold levels. 2. The receiver is locked to the incoming signal 3. The RX Byte alignment is correctly established.
RBC[1:0]	Output	Differential Double Data Rate Recovered Clock Output
RX_ERROR	Output	A high on RX_ERROR indicates that a data reception error has occurred.

TX Block Signals

Signal Name	Direction	Signal Description
TXP, TXN	Output	Differential Outputs from the PHY
TBC	Input	Transmit Clock Reference. Signals Data on Both Edges.
TX_DATA	Input	Data to be Transmitted. TX_DATA Bus can be 10 bits or 20 bits in size depending on configuration.
TX_ENABLE	Input	Transmit Enable enables the Serial ATA PHY line drivers in the AFE portion of the PHY. When it's high, the bits on TX_DATA are used to generate normal driving levels on TXP, TXN pins. When it is low, TXP, TXN outputs are idle and maintain common mode bias as specified in Serial ATA specification.

OOB Block Signals

SIGNAL_LEVEL_VALID	Output	Signal Detect. This output signal from the PHY indicates that the differential input on RXP, RXN pins exceeds the Squelch detector threshold. This signal is functional even without REF_CLK so it can be used as an indication for wake-up from a suspended state.
COMWAKE_DETECT	Output	COMWAKE detected on the line
COMINIT_DETECT and/or COMRESET_DETECT	Output	COMINIT and/or COMRESET detected on the line
COMSAS	Output	COMSAS signaling has been detected on the line.

Control Signals

REF_CK	Input	Reference Clock Input to the PHY Nominal Value of Reference Clock is 100 MHz. 50 MHz can be supported if required. Other speeds are also supported.
PARTIAL	Input	When high places PHY in Partial Power State as defined by Serial ATA specification. The clock output from the PHY will be high during Partial Power State.

SLUMBER	Input	When high places PHY in Slumber Power State as defined by Serial ATA specification. The clock output from PHY will be inactive during Slumber Power State but Out-of-Band Signaling Detectors will continue to function.
RESET	Input	Reset all PHY internal state to its default condition
DATA_RATE	Input	Selects Data Signaling rate Between Gen1 (low) and Gen2 (high)
NEARLB	Input	**Optional** loops back Transmitted Data to its Receive Path
FARLB	Input	**Optional** Loops back Received Data to its Transmit Path

ASIC Clock Generation Signals

ASIC_CK	Output	ASIC Clock generated by the PHY. 150 MHz for Gen1 speed and 150 or 300 MHz for Gen2 Speed. Controlled by ASIC_CK_RATE_SELECT input signal.
ASIC_CK_RATE_SELECT	Input	Selects between 150 MHz or 300 MHz ASIC_CK output. A low level produces 150 MHz and a high level produces 300 MHz.

Vendor Specific Signals

VSP[13:5]	Output	Vendor Specific Output Pins
VSP[4:0]	Input	Vendor Specific Input Pins
VSP Pins are used to control Various Options in the PHY. One Documented VSP Option is the selection of the REF_CK input frequency Option. SMS6000 Supports 50 MHz, 100 MHz, 125 MHz, and 250 MHz REF_CK input speeds and this option can be selected with VSP Access.		

Signal Timing

PHY Output Timing			
	Min	**Max**	**Units**
GEN1_RX_DATA_SETUP	3.0	-	ns
GEN1_RX_DATA_HOLD	0.3	-	ns
GEN2_RX_DATA_SETUP	1.8	-	ns
GEN2_RX_DATA_HOLD	0.3	-	ns

Transmit Timing			
	Min	**Max**	**Units**
GEN1_TX_DATA_SKEW	-1.5	+1.5	ns
GEN1_TX_DATA_DELAY	5 Gen1 bit times – 1.5ns	5 Get1 bit times + 1.5ns	
GEN2_TX_DATA_SKEW	-0.75	+0.75	ns
GEN2_TX_DATA_DELAY	5 Gen2 bit times – 0.75ns	5 Gen2 bit times – 0.75ns	