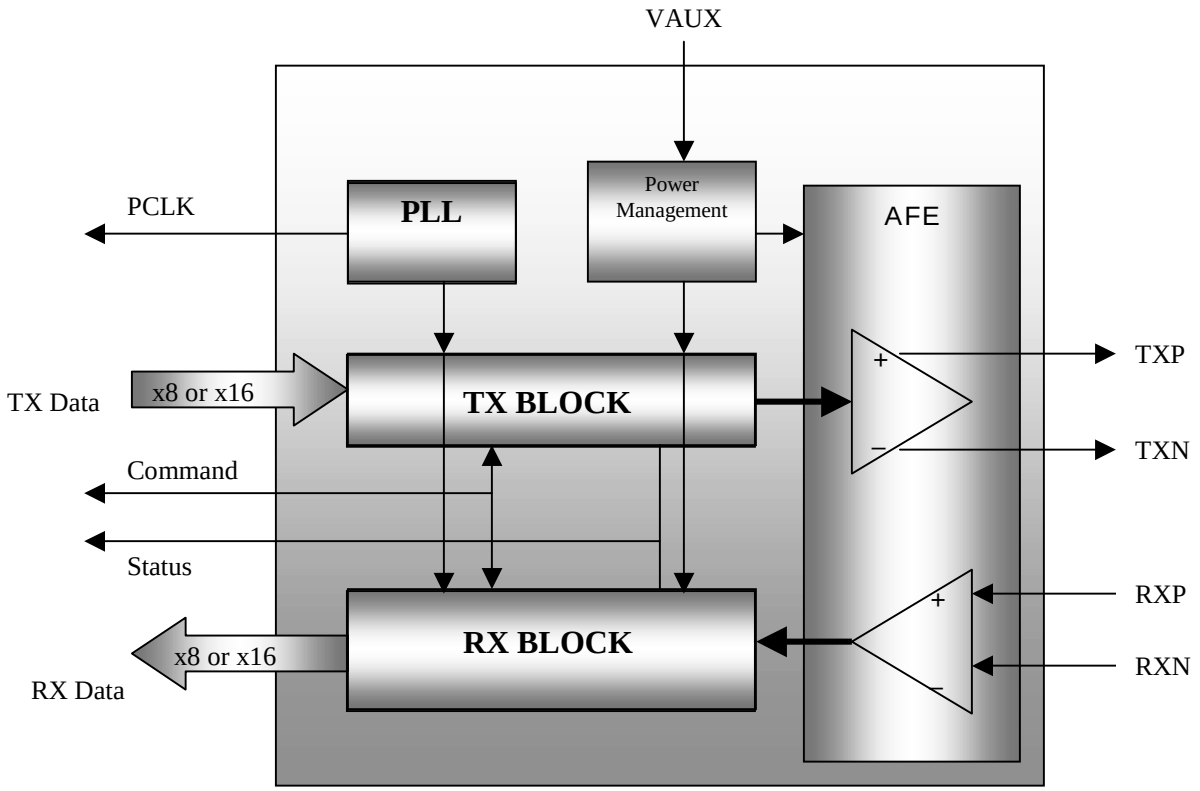
# SMS5000 PCI-Express PIPE PHY TRANSCEIVER

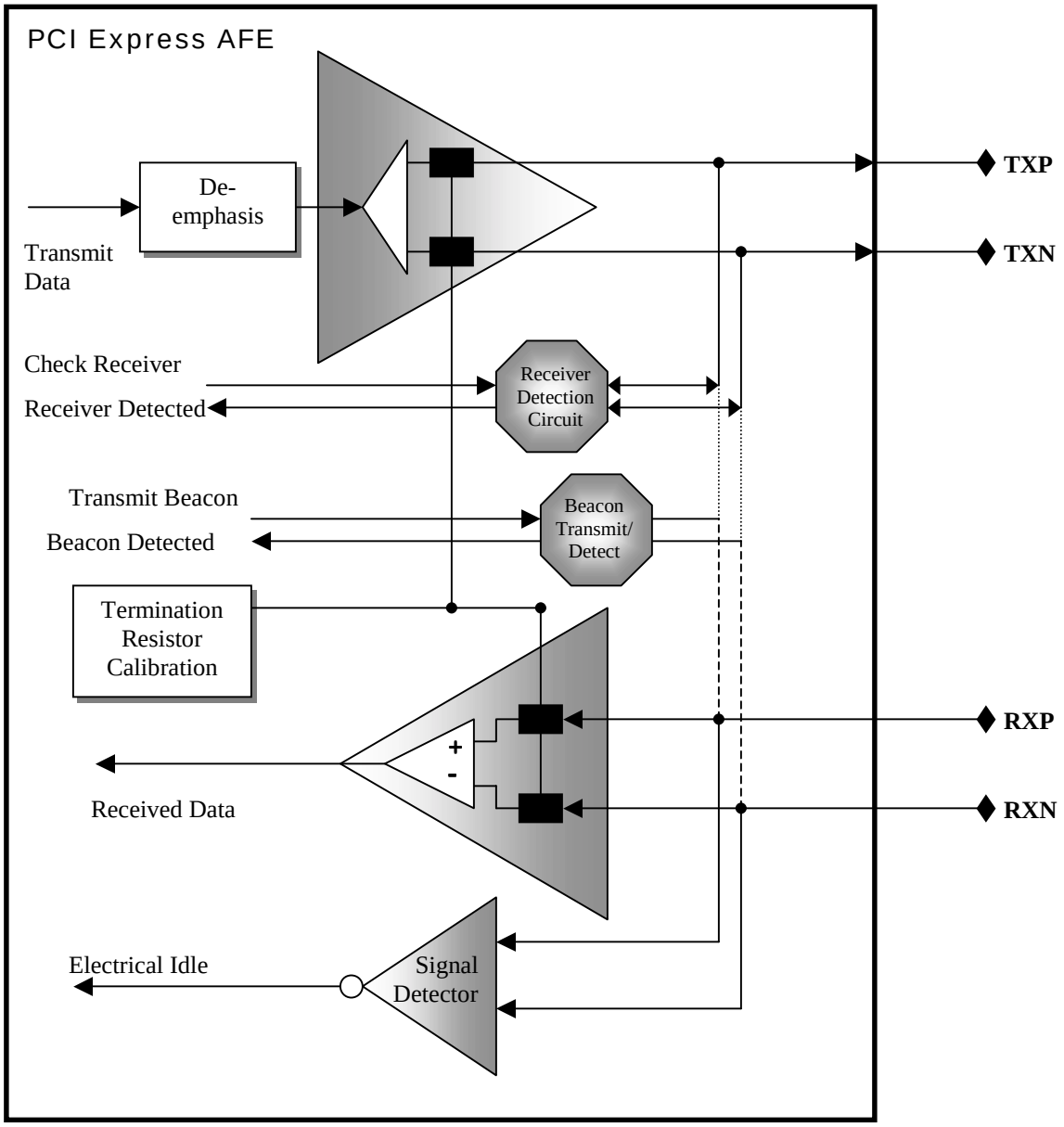



## MAIN FEATURES

- Supports 2.5Gb/s serial data rate
- Utilizes 8-bit or 16-bit parallel interface to transmit and receive PCI Express data
- Full Support for Auxiliary Power (Vaux) for Energy aware systems like Multi-Port Host Controllers
- Data and clock recovery from serial stream on the PCI Express bus
- Supports direct disparity control for use in transmitting compliance pattern
- 8b/10b encode/decode and error indication
- Receiver detection
- De-emphasis at Transmit
- Electrical Idle Generation & Detection
- Lane Polarity Inversion Support
- Loop-back Support
- Spread Spectrum Clock Support
- Embedded Bit Error Rate Testing Through PBRS generation and detection
- ESD & Short Circuit Protection
- Scrambling Disable Feature
- Beacon transmission and detection
- Direct Disparity Control Support for use in transmitting compliance pattern
- Full low cost, low power CMOS Implementation
- Modular architecture supports 2,4,8,16 Lane applications
- Silicon Optimized, Proprietary architecture yields very small silicon area
- Hot Swap, Hot Plug Support

**SMS5000** is a fully integrated CMOS transceiver that handles the full Physical Layer PCI Express protocol and signaling. It contains all necessary AFE (Analog Front End), Clock synthesis, Clock Recovery, Serializer, De-serializer, Comma detect for 8B/10B encoded data and frame alignment functionalities. Digital controller interface is realized with a 8-bit parallel operation (Optional 16-bit Interface) that allows use of 250 MHz reference Clock. The transceiver includes Receiver Detection, Beacon Generation, Beacon Detection and Signal Detect capability compliant with PCI Express Specification requirements and provides Short Circuit Protection to ground for outputs. **SMS5000** also includes calibrated Transmitter and Receiver Termination Resistors compliant with the requirements of the PCI Express Base 1.0a Specification.

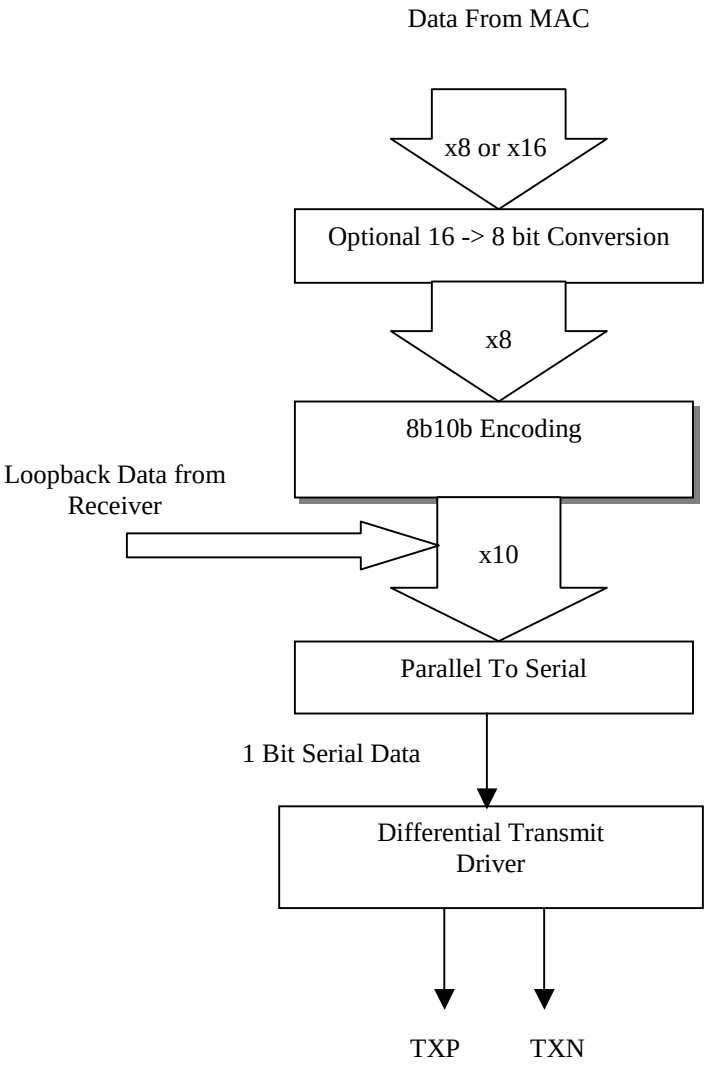
**SMS5000** does not require any external Loop filter capacitor(s) for clock Synthesis PLL or Clock recovery circuitry making it immune to PCB related noise typically encountered, and provides a completely integrated solution.



## Transmit Block:

Transmitter Block includes 8b/10b Encoder, Parallel To Serial Converter and Transmit Differential Driver. Also included in the transmitter block are the Loopback support functionality, transmit running disparity negation for compliance testing and receiver detection support.

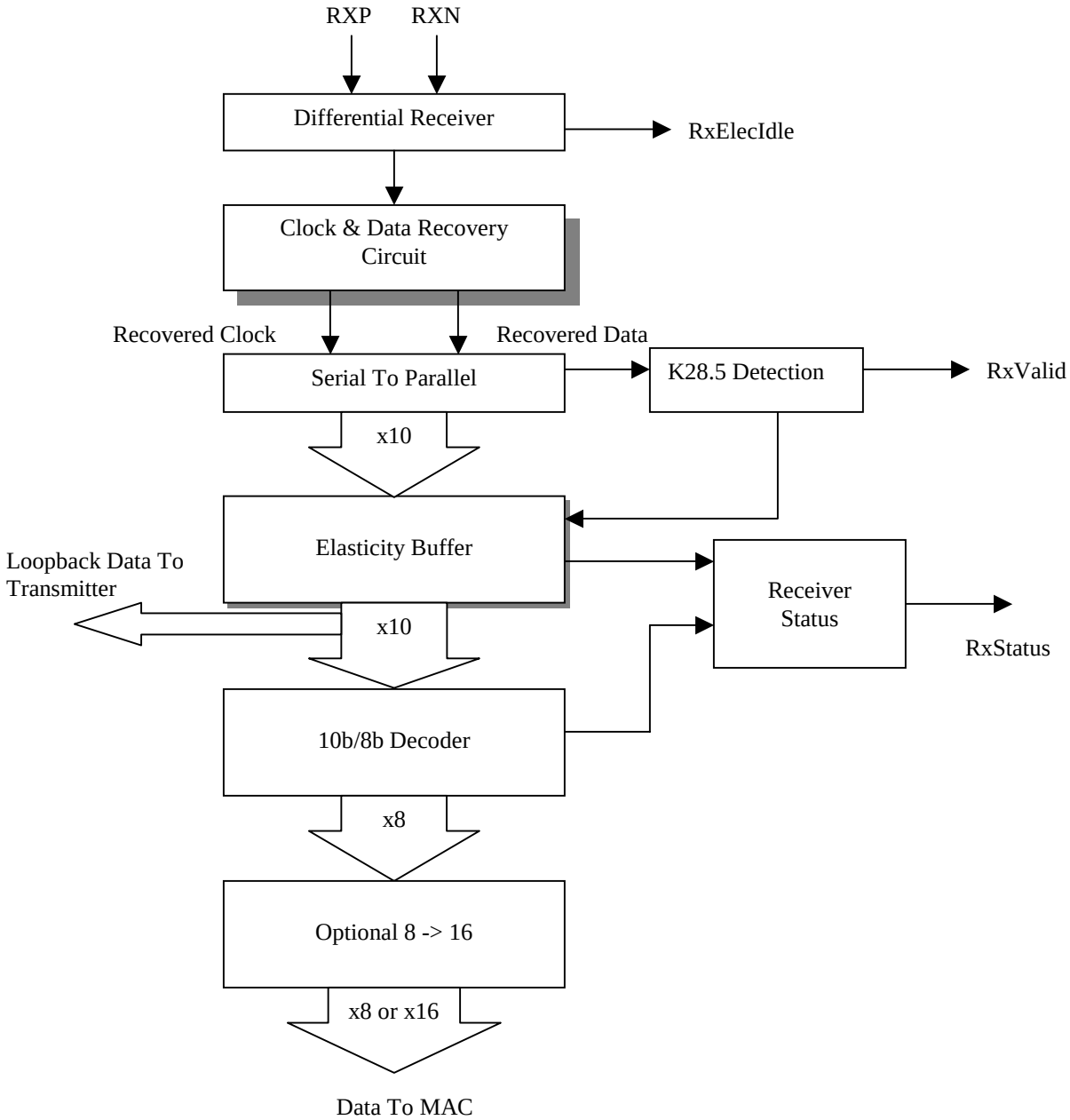
When TxElecIdle is not active, the transmit path takes either 8-bit data from the MAC over TxData and TxDataK busses. There is an optional 16-bit input conversion. Data to be transmitted goes through an 8b/10b encoding compliant with the PCI Express Base Specification. If Loopback is enabled, the data to be transmitted comes from the Receive path instead of the MAC Interface. Then the parallel data is converted to serial and driven through the AFE TX Driver block on to the PCI Express Channel via the TXP, TXN pins.



## Receiver Block:

Receiver Block includes Differential Receiver, Clock and Data Recovery Blocks, Comma Detect Circuit, Bit and Symbol Alignment, Serial To Parallel Converter, Elasticity Buffer, 10b/8b Decoder with Optional 16-bit Output. 10b/8b decoder also supports code and Parity error detection to report to the link layer.

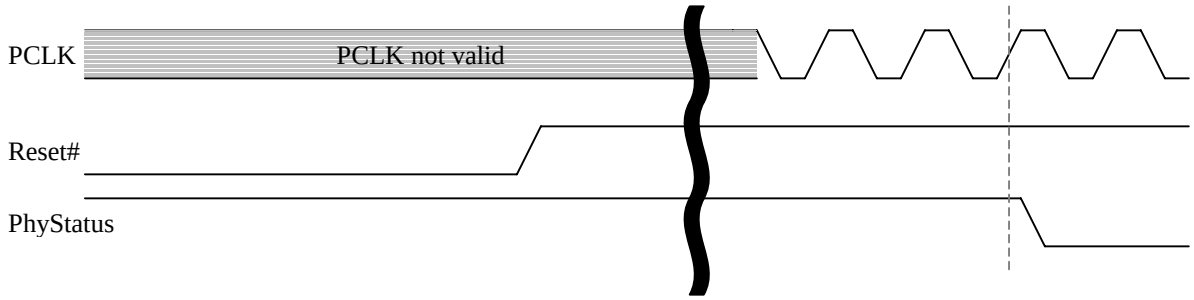
The Receive Block takes its input from the RXP, RXN pins. The differential Receiver in AFE in cooperation with the signal detect block in AFE converts this into a digital signal. The Clock and Data Recovery circuit detects the edge change times of the received data and adjusts its sampling phase to recover the correct bits from the PCI Express channel. Then the recovered data is converted to parallel form, and COMMA detect circuit detects the K28.5 COMMA symbols and aligns the received 10 bit word to be processed in Elasticity Buffer. The ouput of the Elasticity Buffer is also sent to the Transmit path for Loopback purposes. The Receive Status is decided from the Elasticity Buffer state and the following 10b/8b decoder state. After 10b/8b decoding, the parallel data is optionally converted to 16 bits and given to the MAC on the RxData, RxDataK interface.



## PHY Functional Behavior:

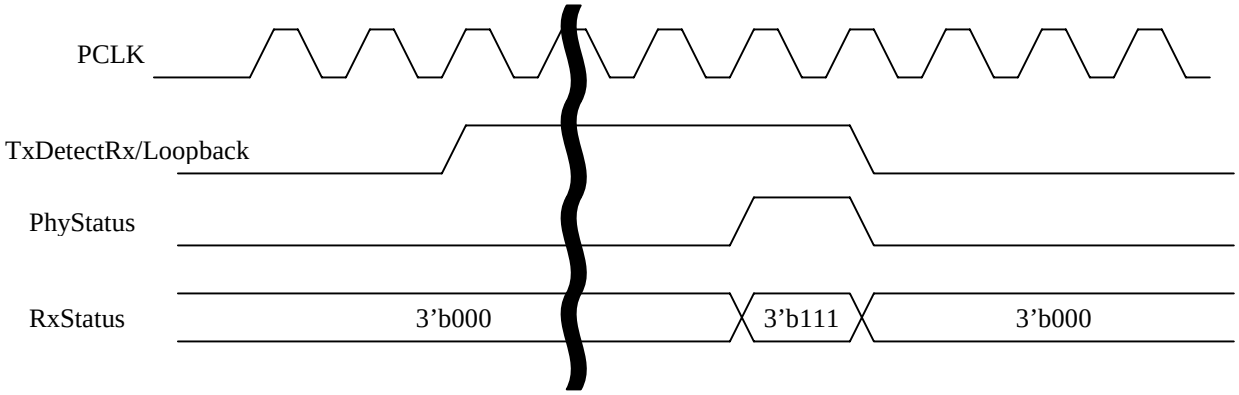
### Reset:

When the MAC wants to reset the PHY, it needs to assert it until power and clock to the PHY are stable. The PHY signals the MAC that the PCLK is stable by de-asserting PhyStatus.




### Receiver Detection:

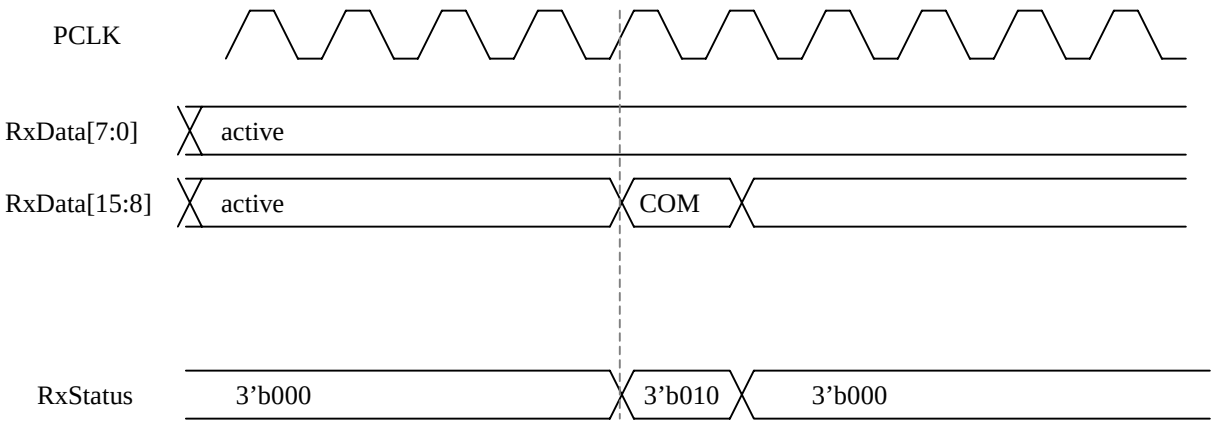
While the PHY is in P1 state, it can be instructed to perform a receiver detection operation to check if there is a receiver on the other side of the link. To do a receiver detection operation, the MAC asserts the TxDetectRx/Loopback signal. When the PHY completes the receiver detection operation, it asserts the PhyStatus for one clock and drives the RxStatus with the appropriate value. After the PHY signals the end of the receiver detection operation by asserting the PhyStatus, the MAC should de-assert TxDetectRx/Loopback signal.




### Clock Frequency Difference Compensation:

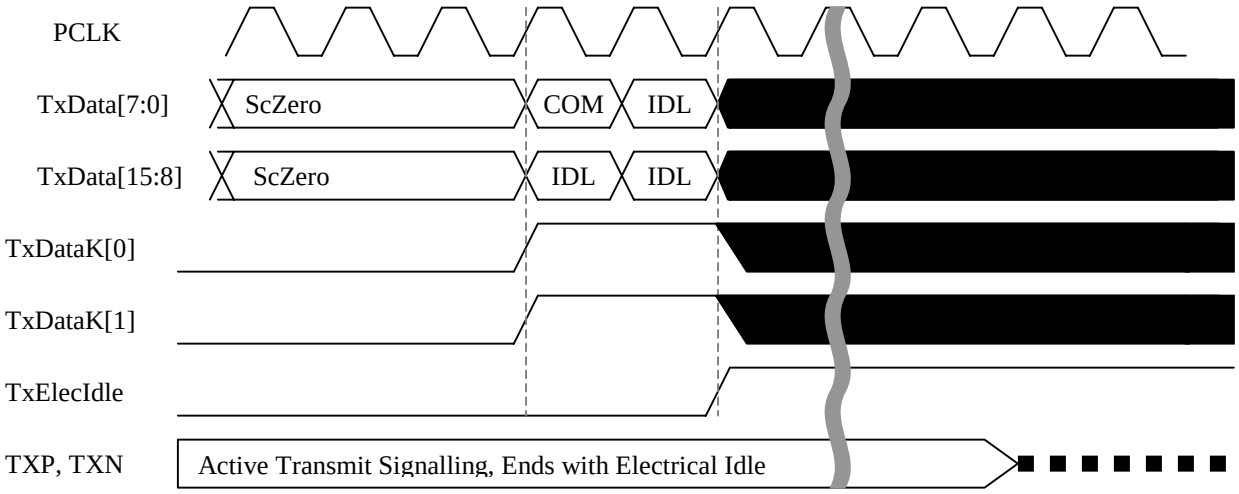
The frequencies of the two sides of a link can be different up to a maximum of 600 ppm and the receiver PHY includes an elasticity buffer to compensate the bit rate difference caused by this. The PHY accomplishes this by inserting and removing SKP symbols into the received data stream to prevent the elasticity buffer from underflowing or overflowing. Whenever the PHY adds or removes a SKP symbol from a SKP ordered-set, it notifies the MAC by signaling this action on the RxStatus[2:0] signals.

In the figure below, the deletion of a SKP symbol is indicated




**Electrical Idle:**

PCI Express Base Spec requires that devices send an Electrical Idle ordered set before TXP, TXN goes to the electrical idle state.



# PIPE Interface Specification

Transmit Data Signals

| Name | Direction | Active Level | Description |
|---|---|---|---|
| TXP, TXN | Out | n/a | Differential Outputs from the PHY. |
| TxData | In | n/a | Parallel Input data bus to the PIPE PHY. It can be 16 bits or 8 bits in size. |
| TxDataK | In | n/a | Data/Control Signal for Data bus into the PIPE PHY. For 16 bit data bus, it is 2 bits in size. Bit 0 indicates control for low byte of TxData and Bit 1 indicates control for high byte. For 8 bit data bus, TxDataK is single bit. A 0 value indicates a data byte and a 1 value indicates a control byte. TxData & TxDataK signals are valid when the PHY is in P0 power state and TxElecIdle is inactive |

Receive Data Signals

| Name | Direction | Active Level | Description |
|---|---|---|---|
| RXP, RXN | In | n/a | Differential Inputs to the PHY. |
| RxData | Out | n/a | Parallel Output data bus from the PIPE PHY. It can be 16 bits or 8 bits in size. |
| TxDataK | Out | n/a | Data/Control Signal for Data bus from the PIPE PHY. For 16-bit data bus, it is 2 bits in size. Bit 0 indicates control for low byte of RxData and Bit 1 indicates control for high byte. For 8-bit data bus, RxDataK is single bit. RxData & RxDataK signals are valid RxValid output signal is active high |

Command Signals

| Name | Direction | Active Level | Description |
|---|---|---|---|
| TxDetectRx /Loopback | In | High | Differential Inputs to the PHY. |
| TxElecIdle | In | High | Forces PHY TX Output to Electrical Idle when asserted<br>• When deasserted in P0 state, indicates that there is valid data in TxData and TxDataK pins.<br>• When deasserted in P2 state, indicates that the PHY should transmit Beacon signaling.<br>TxElecIdle should always be asserted in P0s and P1 states. |
| TxCompliance | In | High | Sets the transmit running disparity to negative. It's used when transmitting the compliance pattern |
| RxPolarity | In | High | If High, it tells the PHY to do a polarity inversion on the received data. |
| Reset# | In | Low | Resets the transmitter and receiver and all internal states of the PHY. This signal is asynchronous. |
| PowerDown[1:0] | In | n/a | Controls the Power Down mode of the PHY<br>[1] [0] Description<br>0 0 P0, normal operation state<br>0 1 P0s, low recovery latency power saving<br>1 0 P1, longer recovery, lower power<br>1 1 P2, lowest power state |

Status Signals

| Name | Direction | Active Level | Description |
|---|---|---|---|
| RxValid | Out | High | Indicates bit lock, symbol lock and valid data on RxData(K) |
| PhyStatus | Out | High | Indicates completion of several PHY functions. |
| RxElecIdle | Out | High | Indicates Receiver Detection of an Electrical Idle. |
| RxStatus[2:0] | Out | n/a | Encodes Receiver Status and Error Codes<br>[2] [1] [0] Description<br>0 0 0 Received Data OK<br>0 0 1 1 SKP Removed<br>0 1 0 1 SKP Added<br>0 1 1 Receiver Detected<br>1 0 0 8b/10b Decode Error<br>1 0 1 Elasticity Buffer Overflow<br>1 1 0 Elasticity Buffer Underflow<br>1 1 1 Receive Running Disparity Error |

External Signals

| Name | Direction | Active Level | Description |
|---|---|---|---|
| CLK | In | Edge | Reference clock for the PHY PLL, 50 MHz or 100 MHz supported (125 MHz, 250 MHz optional) |
| PCLK | Out | Pos Edge | PHY Parallel Interface clock for TxData(K) and RxData(K) and associated control signals. For 8 bit data interface this clock is 250 MHz and for 16-bit data interface, it is 125 MHz. The positive edge is used as reference. |

## Timing Parameter Specification (Preliminary)

| Timing Parameter | Description | Unit | Typical | Worst |
|---|---|---|---|---|
| Transmit Latency | Time for data moving between the parallel interface and the PCI Express serial Lines. | ns | tba | 20 |
| Receive Latency | Time for data moving between the PCI Express serial Lines and the parallel interface | ns | tba | 50 |
| Loopback Enable Latency | Amount of time it takes the PHY to begin looping back received data. | ns | tba | 20 |
| Transmit Beacon | Time from when MAC directs the PHY to send a beacon until the beacon signaling begins at the serial pins. | ns | tba | 20 |
| Receive Beacon | Timed from when valid beacon signaling is present at the receiver pins until RxElecIdle is deasserted. | ns | tba | 80 |
| N_FTS with common clock | Number of FTS ordered sets required by the receiver to obtain reliable bit and symbol lock when operating with a common clock | ns | tba | tba |
| N_FTS without common clock | Number of FTS ordered sets required by the receiver to obtain reliable bit and symbol lock when operating without a common clock. | ns | tba | tba |
| PHY Lock Time | Amount of time for the PHY receiver to obtain reliable bit and symbol lock after valid TSx ordered-sets are present at the receiver. | ns | tba | tba |
| P0s to P0 transition time | Amount of time for the PHY to return to P0 state, after having been in the P0s state. | ns | tba | Tba |
| P1 to P0 transition time | Amount of time for the PHY to return to P0 state, after having been in the P1 state. | ns | tba | Tba |
| P2 to P1 transition time | Amount of time for the PHY to return to P1 state, after having been in the P2 state. | ns | tba | Tba |
| Reset to Ready Time | Timed from the when RESET# is deasserted until the PHY de-asserts PhyStatus | ns | tba | 200 |